WHAT IS CLAIMED IS:

1. An integrated circuit fabrication process, the process comprising the steps of:

patterning a transistor gate pattern on a photoresist layer;

curing the transistor gate pattern with an electron beam;

trimming the cured transistor gate pattern; and

transferring the trimmed transistor gate pattern to a layer disposed below the photoresist layer to form a transistor gate, wherein the transistor gate includes a width and a length, and a variation of the width along the length of the transistor gate is reduced due to the curing step.

2. The process of claim 1, wherein the photoresist layer is comprised of a photoresist material typicaly used for at least one of 248 nm lithography, 193 nm lithography, and extreme ultraviolet light (EUV) lithography.

3. The process of claim 2, wherein the photoresist layer is comprised of a photoresist material of a type typically used for 193 nm and 248 nm lithography and is commercially available.

4. The process of claim 1, wherein the final gate transistor width is in the range of approximately 20-60 nm.

5. The process of claim 1, wherein the curing step includes exposing the transistor gate pattern to the electron beam having a dose in the range of approximately 100-100000 $\mu C/cm^2$.

6. The process of claim 1, wherein the curing step includes exposing the transistor gate pattern to the electron beam having an accelerating voltage in the range of approximately 0.5-20 Kv.

7. The process of claim 1, wherein the curing step includes changing at least one of a vertical etch rate, a horizontal etch rate, and a minimum extension erosion rate associated with the transistor gate pattern.

8. A method of forming a transistor having a gate width of less than 70 nm, the method comprising the steps of:

E-beam radiating a gate pattern of a photoresist layer;

trimming the E-beam eradiated gate pattern of the photoresist layer; and

etching a polysilicon layer disposed below the photoresist layer in accordance with the trimmed gate pattern to form a gate of the transistor, the gate width being less than 70 nm.

9. The method of claim 8, wherein the E-beam radiating step uses an electron beam at a dose in the range of approximately 100-100000 $\mu C/cm^2$.

10. The method of claim 9, wherein the electron beam is provided at an accelerating voltage in the range of approximately 0.5-50 Kv.

11. The method of claim 9, wherein a uniformity of the gate width is 4 to 6 nm over 3 nm segment.

12. The method of claim 9, wherein the photoresist layer is comprised of a material selected from a group including acrylate-based polymer, alicyclic-based polymer, and phenolic-based or polystyrene-based polymer.

13. The method of claim 9, wherein the E-beam radiation step includes affecting at least one of a vertical etch rate, a horizontal etch rate, and a minimum extension erosion rate associated with the gate pattern of the photoresist layer.

14. The method of claim 9, wherein the E-beam radiation step achieves an enhancement interim rate for a commercially availabe resists

using lithography processes with either 248 nm and 193 nm wavelength of light.

15. An integrated circuit, comprising:

an isolation region;

a transistor surrounded by the isolation region, wherein the transistor includes a gate, a critical dimension of the gate being less than approximately 60 nm, and the gate being defined by an E-beam eradiated gate feature on a photoresist layer.

16. The integrated circuit of claim 15, wherein the E-beam eradiated gate feature on the photoresist layer is formed by an electron beam exposure.

17. The integrated circuit of claim 15, wherein a uniformity of the critical dimension along a length of the gate is 4 to 6 nm over a 3 nm segment.

18. The integrated circuit of claim 15, wherein the photoresist layer is comprised of a material selected from acrylate-based polymer, alicyclic-based polymer, and polystyrene and phenolic-based polymer.

19. The integrated circuit of claim 18 wherein the critical dimension is between 20 and 60 nm.

20. The integrated circuit of claim 18 wherein uniformity of the critical dimension along a length of the gate is 4 to 6 more a 3 nm segment.